Next Generation Metallization Technique for IC Package Application

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ABSTRACT

IC package substrates are normally fabricated by semi-additive process (SAP) for high-density packaging. Dow's brand new Ni-free electroless copper chemistry developed for SAP offers new solutions for the future fine pattern design to IC substrate production. The new developed chemistry shows high productivity (0.6um/20min) and peel strength (over 0.5kN/m on 100nm roughness) and improved micro via holes (MVH) uniform deposition with no Cu-Cu connection defects.

INTRODUCTION

IC package market is significantly growing driven by increased demand of mobile electronics and network infrastructure. Due to improvement of processing speed and frequency, IC chip assembly is shifting from wire bonding to "Flip-Chip" to miniaturize and integrate IC package. [1]
In terms of electroless copper in SAP, high peel strength on low surface profile material, high Cu-Cu joint reliability and high productivity with long bath life are strongly required. Moreover, for the further fine circuit pattern design, MVH covering performance with thinner deposit thickness on the dielectric surface deliver more flexible fine pitch patterning design. Also, environmental friendly chemistry is preferable from the environmental aspects.

Currently in SAP market, use of Ni-Cu deposited film is common approach for higher deposition rate, higher peel strength and smooth surface morphology. [2] However, Ni-Cu deposition system still remains some issues. For instance, Ni-containing electroless copper film can't be removed efficiently by flash etching process, which causes the side-etch and under-cut issues. Use of Ni-Cu co-deposited system will limit further fine circuit pattern design in the future.

In this paper, the performance of the novel Ni-free erelctroless copper bath is described. Without Ni, proper selection of functional additives can provide excellent plating performance in terms of deposition rate, peel strength on low profile dielectric, uniform deposition inside the MVH and Cu-Cu joint reliability with great bath stability.

EXPERIMENTAL

Sample preparation

Three kinds of dielectric materials were tested. The surface roughness (Ra) on these dielectric materials were dielectric material A: 300nm, B: 100nm and C: 80nm after DOW's desmear treatment.

Deposition thickness

The deposited thickness was measured on bare FR4 by SFT9450 X-ray fluorescence (XRF) spectroscopy made by SII nano technology.

Peel strength

25um of acid copper was applied to the electroless copper surface to measure the peel strength. 5564 Tensile Test machine made by INSTRON Japan Co.,Ldt was used for peel strength measurement. The peeling speed was 50mm/min, and the sample width was 10mm.

Uniform deposition in micro via holes

Electroless copper deposit uniformity was evaluated based on cross-section observation. MVH with 50um in diameter and 35um in depth were evaluated.

Cu-Cu joint reliability

Same of the MVH for deposit uniformity evaluation were used after applying Cu filling process.

All the chemicals such as cleaner, catalyzer and reducer were Dow Electronic Materials commercialize products. The condition of electroless copper plating was at 32 degree C. The electoless copper thickness was around 0.6 μ m at 20minitutes of plating time.

RESULTS AND DISCUSSION

Deposition behavior

Controlling deposition behavior is one of the key techniques to obtain not only high productivity but also high peel strength. Our new developed chemistry has unique characteristics in deposits behavior. Generally the deposition reaction can be divided into two phases. The first is initial deposition phase which occurs on palladium, and the second occurs on deposited copper by autocatalytic reaction. In general electroless copper bath, the deposition rate tends to be faster in the first 10 minutes, then the deposition rate gets slower. Finally the deposition reaction becomes inactive. This conventional deposition behavior has some critical issues. When the initial deposition is relatively fast, the deposited copper crystal can't follow the dielectric surface profile which leads to poor peel strength as a consequence of generated micro void in the vicinity of dielectric. Another issue is decreased deposition rate at the second phase which limits the productivity. Overcoming these challenges in general electroless copper bath, Dow has found out an additive having significant feature which makes an impact on deposition behavior. In the first 10minutes, the additive work as a deposition suppressor to obtain the uniform deposits following the dielectric surface profile and cover the palladium seeds completely, and after 10 minutes plating, the deposition rate gets faster lineally for high productivity.(Fig.1)

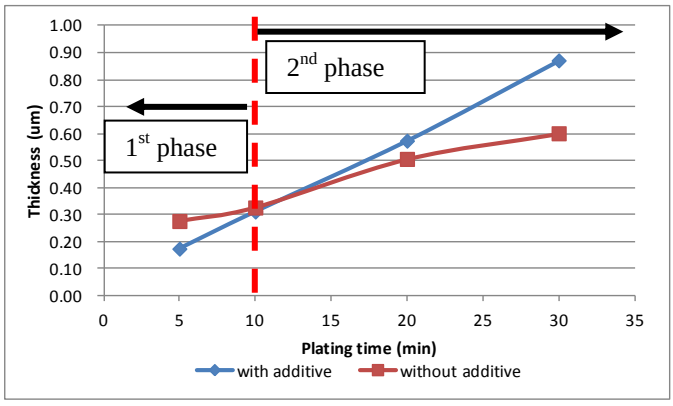

Figure 1: Deposition behavior with and without Dow's additive

Observation of surface morphology by Scanning electron microscope (SEM) revealed that the plated film from the bath with Dow's additive closely follow the structure of the dielectric material as shown in Fig.2-A. In contrast, the plated film without the additive is not following the structure of dielectric materials as showing in Fig.2-B. It seems that the deposited crystallites easily combine with adjacent crystal which generates a lot of micro voids. The difference in deposition performance is considered to cause different peel strength.

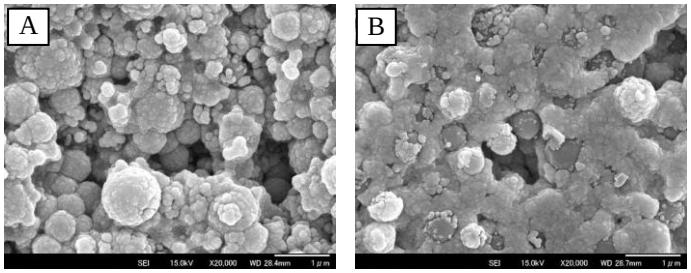

Figure2: SEM images of initial deposited crystal
(A): with Dow new additive (B): without additive

Peel strength

It's been challenging to obtain high peel strength on low roughness dielectric [3]. Although the smooth surface is necessary for reducing the interconnection delays and increasing whole performance, the difficulty is to create high adhesion onto such smooth surface. Our newly formulated product with Dow's additive showed excellent and stable peel strength on various dielectric materials. Fig.3 indicates excellent peel strength on major dielectric materials for IC package.

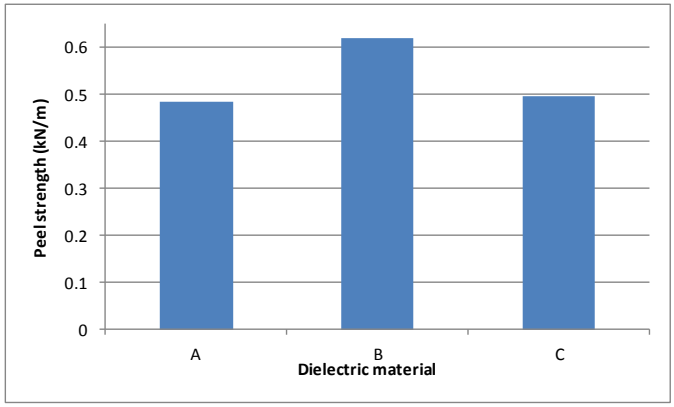

Figure3: Peel strength on various dielectrics

After 90 degree peel test, the surface of copper plated side and dielectric resin side were observed with SEM. Fig.4 exhibits the surface morphology of copper plated side. In case of using Dow's additive, plenty of resins which came from dielectric materials were observed as shown in Fig.4-A. In contrast, only a few resins were observed without the additive. Moreover, observation of resin side surface shows some trace of removed resins in Fig.5-A.

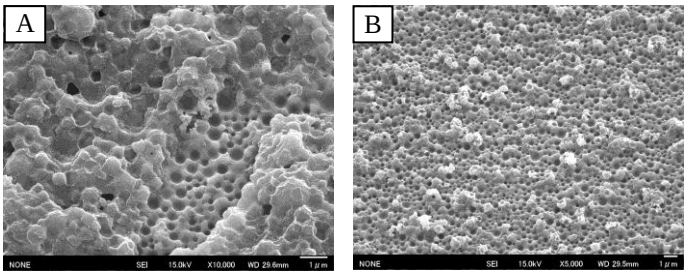

Figure4: SEM images of surface morphology on copper plated side
(A): with additive, (B) without additive

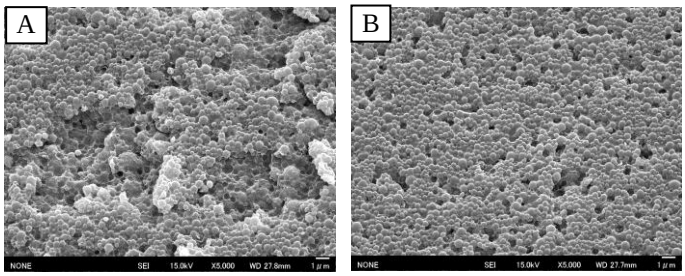

Figure5: SEM images of surface morphology on resin side
(A): with additive, (B) without additive

In addition to the surface observation, X-ray photoelectron spectroscopy (XPS) analysis was applied in order to investigate the fracture mode at the atomic level. The surface at the atomic level can be probed with good accuracy using XPS analysis. In XPS analysis, fracture surface of both copper plated side and resin side were analyzed. The analysis results shown in Table1 reveal that more Pd was detected on the copper plated side with additive included bath, compared to without the additive deposits. These observations and analysis results suggest that the failure mode of plated film with additive was cohesive failure and that of plated film without additive was interfacial failure. This means that the use of additive can form high adhesive layer onto the dielectric material.

Table1. XPS analysis on fracture surface (at. %)

	Copper plated side		**Resin side**	
	With additive	Without additive	With additive	Without additive
C	69.4	64.3	70.5	58.5
O	16.3	16.5	20.4	26.6
Si	4.5	N.D.	6.6	12.6
Cu	6.8	13.4	0.4	0.44
Pd	0.14	0.62	N.D.	N.D.

Fig.6 depicts the peel strength which was obtained from different plating thickness. The electroless copper thickness was varied from 0.40um to 0.87um. Our new product with Dow's additive is capable to obtain consistent peel strength on thinner deposit thickness. Since the peel strength value is independent of the plating thickness, it seems that this result showed even thinner plating has high quality deposits layer. The thin thickness helps form the fine circuits patterning, since thinner thickness will be preferable in the flash etching process to minimize the side–etching issue. In terms of peel strength, our new product contributes the fine pattern design required in the future.

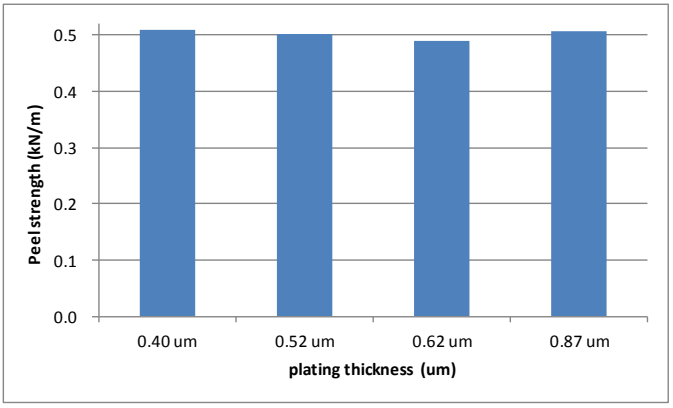

Figure6: Peel strength on several plating thickness

Uniform deposition in micro via holes

High deposition uniformity inside MVH is also a key performance for not only following MVH filling but also the further fine pattern design which requires thinner deposit on the dielectric surface. In terms of uniform deposition inside MVH, our new product achieves over 80% of throwing power with addition of Dow's new additive as shown in Fig.7-A.

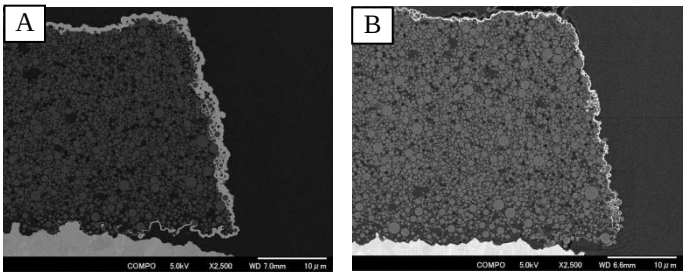

Figure7: SEM images of uniform deposition inside MVH
(A): with additive, (B) without additive

In general, essential components such as copper tend to be deficiency inside the MVH during plating, and this shortage causes inactive plating reaction, especially on the MVH bottom.[4] One of the solutions for this issue is to agitate strongly to feed necessary components into the MVH. Our new additive has an important role in the plating reaction inside the MVH. Fig.8 shows the deposit thickness plated with several copper concentration baths. The copper concentration in the baths was varied from 40% to 100%. As shown in Fig.8, the additive can accelerate the plating reaction under shortage of copper concentration. Our new additive delivers much copper deposits under less copper concentration, and this characteristic provides high MVH covering performance.

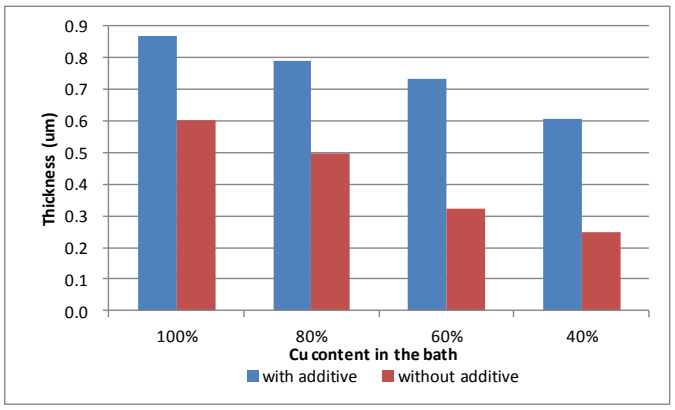

Figure8: The deposit thickness with several copper contents

Copper-Copper joint reliability

Copper-copper joint reliability was evaluated by Quick Via Pull (QVP) test. The following table2 shows the QVP results. As shown in table2, new product with Dow's additive achieved 100% pass rate. Moreover, some voids were observed at the bottom of the film without additive as shown in Fig.9-B. These results suggest that the film plated with new additive has good Cu-Cu joint reliability, while the plated deposits without additive has potential of failure structure formation.[5] This high reliability will ensure the copper-copper connection with smaller via hole which has smaller bottom area.

Table2. The result of QVP test with and without additive

	Pass	Failure
With additive	100%	0%
Without additive	25%	75%

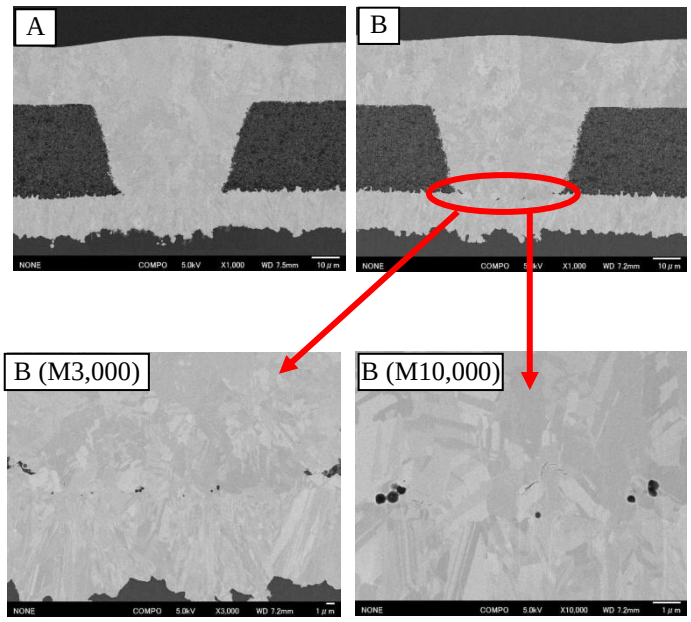

Figure9: Observation of voids around MVH bottom
(A): with additive, (B) without additive

Patterning design capability

The electroless copper deposition is mainly to give conductive layer to the dielectric materials. Eventually the unnecessary electroless copper layer needs to be removed in the flash etch process. In flash etch process, the electroless copper layer should be removed easily in order not to give damages to the circuit pattern. In some mass production, Ni-Cu deposited layer is employed. However typical Ni-Cu deposited layer isn't easy to be removed in flash etching process which leads to serious damage to plated pattern during flash etching process. Therefore in case of Ni-Cu deposited system, the fine patterning design will be highly limited due to the negative impact of the flash etch process. One of the key technologies for fine pattern achievement is removing only unnecessary deposits in order to minimize the circuit pattern damages. As we discussed in this paper, our new formulation achieves outstanding performance without addition of Ni, and that layer is easily removed by etching chemical. Fig.10 shows the comparison of etching time in deposited film with and without Ni. The figure indicates the Ni included deposits needs longer time for etching, and this implies that the etching chemical needs to be stronger to remove Ni-Cu deposits. As a consequence of this strong etching condition, the formed pattern will get narrow; so called side etch, and the pattern should be designed as a result of large negative side-etch. In order to provide design flexibility, Dow's pure Cu deposits system with new additive can overcome the pattern design issues for fine pattern fabrication.

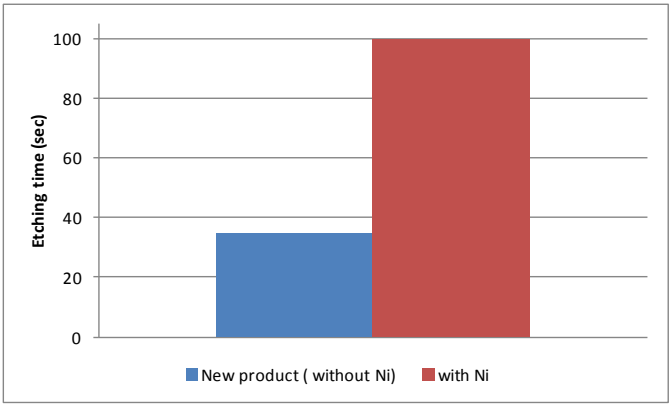

Figure10. Comparison of each deposits film on etching time

CONCLUSION

Novel electroless copper product has been developed in order to contribute the further fine pattern technique in IC package segments. In all evaluation items, the brand new product with new additive demonstrates excellent performance. In addition to basic performance, the high peels strength regardless of its electorless copper thickness, high throwing power and Ni free pure Cu deposits system can contribute to further fine pattern design required in the near future.

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